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41 VHDL-based design and design methodology for reusable high performance direct digital requency synthesizers
Ireneusz Janiszewski, Bernhard Hoppe, Hermann Meuth
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(226.11 KB) Additional Information: full citation, abstract, references, index terms

Design methodologies for high performance Direct Digital Fre-quen--cy Synthesizers (DDFS) are described. Traditional look-up tab-les (LUT) for sine and co-sine are merged with CORDIC-inter-po---la--tion into a hybrid architecture. This implements DDFS-sys-tems with high resolution without being specific to a particular tar-get technology. Amplitude constants were obtained from ma-the-matical trigonometric functions of the IEEE math_real pack-age. These constants were then written via simula ...

Keywords: CORDIC algorithm, HDL-based design, design optimization and reuse, direct frequency synthesis

42 A transaction-based unified simulation/emulation architecture for functional verification
Murali Kudlugi, Soha Hassoun, Charles Selvidge, Duaine Pryor
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(201.24 KB) Additional Information: full citation, abstract, references, citings, index terms

A transaction-based layered architecture providing for 100% portability of a C-based testbench between simulation and emulation is proposed. Transaction-based communication results in performance which is commensurate with emulation without a hardware target. Testbench portability eliminates duplicated effort when combining system level simulation and emulation. An implementation based on the IKOS VStation emulator validates these architectural claims on real designs.

43 NanoFabrics: spatial computing using molecular electronics
Seth Copen Goldstein, Mihai Budiu
May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture**, Volume 29 Issue 2

Full text available: pdf(996.26 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

The continuation of the remarkable exponential increases in processing power over the recent past faces imminent challenges due in part to the physics of deep-submicron CMOS devices and the costs of both chip masks and future fabrication plants. A promising solution to these problems is offered by an alternative to CMOS-based computing, chemically assembled electronic nanotechnology (CAEN).

In this paper we outline how CAEN-based computing can become a reality. We briefly describe rec ...

44 CAD for RF circuits

P. Wambacq, G. Vandersteen, J. Phillips, J. Roychowdhury, W. Eberle, B. Yang, D. Long, A. Demir

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(396.98 KB) Additional Information: full citation, references, citings, index terms

45 High-level design for asynchronous logic

Ross Smith, Michiel Ligthart

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(82.11 KB) Additional Information: full citation, abstract, references, index terms

Asynchronous, self-timed, logic is often eschewed in digital design because of its ad-hoc methodologies and lack of available design tools. This paper describes a complete High Level Design flow for asynchronous circuits based on Register Transfer Level (RTL) VHDL using commercial simulation and synthesis tools. Contrary to previous asynchronous approaches, the proposed RTL methodology closely resembles familiar synchronous design styles.

46 Session 10D: digital and analog test generation: A parametric test method for analog components in integrated mixed-signal circuits

M. Pronath, V. Gloeckel, H. Graeb

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(153.95 KB) Additional Information: full citation, abstract, references

In this paper, we present a novel approach to use test stimuli generated by digital components of a mixed-signal circuit for testing its analog components. A wavelet transform is applied to the response signal of the device under test (DUT). We will show, that in comparison to Fourier transform or no transform at all, particular properties of this transformation are advantageous for mixed-signal test and especially built-in self test.We introduce a new method for test measurement selection based ...

47 Session 8B: embedded systems power management and validation: A data flow fault coverage metric for validation of behavioral HDL descriptions

Qiushuang Zhang, Ian G. Harris

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(65.11 KB) Additional Information: full citation, abstract, references

Behavioral HDL descriptions are commonly used to capture the high-level functionality of a hardware circuit for simulation and synthesis. The manual process of creating a behavioral description is error prone, so significant effort must be made to verify the correctness of behavioral descriptions. Simulation-based validation and formal verification are both techniques used to verify correctness. We investigate validation because formal verification techniques are frequently intractable for large ...

48 Session 4B: high-level design tools for analog circuits: DAISY: a simulation-based high-level synthesis tool for ΔΣ modulators

K. Francken, P. Vancorenland, G. Gielen

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(240.09 KB) Additional Information: full citation, abstract, references, citings

An integrated tool called DAISY (*D*elta-Sigma *A*nalys*i*s and *Sy*nthesis) is presented for the high-level synthesis of ΔΣ modulators. The approach determines both the optimum modulator topology and the required building block specifications, such that the system specifications -- mainly accuracy and signal bandwidth -- are satisfied at the lowest possible power consumption. A genetic-based differential evolution algorithm is used in combination with a fast dedi ...

49 Session 4B: high-level design tools for analog circuits: Verification of delta-sigma converters using adaptive regression modeling

Jeongjin Roh, Suresh Seshadri, Jacob A. Abraham

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(116.40 KB) Additional Information: full citation, abstract, references

A new verification technique for ΔΣ analog-to-digital converters (ADC) is proposed. The ADC is partitioned into functional blocks, and adaptive regression models for each partition are constructed using transistor-level simulation data. Non-idealities in circuit behavior are captured by the adaptive regression technique from the collected data. The algorithms have been implemented in a simulation program ARSIM (Adaptive Regression Simulator), which performs data sampling, model build ...

50 Retargetable compiled simulation of embedded processors using a machine description language

Stefan Pees, Andreas Hoffmann, Heinrich Meyr

October 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 4

Full text available: pdf(4.06 MB) Additional Information: full citation, abstract, references, index terms

Fast processor simulators are needed for the software development of embedded processors, for HW/SW cosimulation systems, and for profiling and design of application-specific processors. Such fast simulators can be generated based on the machine description language LISA. Using this language to model processor architectures enables the generation of compiled simulators on various abstraction levels, assemblers, and compiler back ends. The article discusses the requirements of software devel ...

Keywords: DSP processors, HW/SW cosimulation, compiled simulation, instruction set simulators, machine description languages, processor modeling and simulation, system-on-chip

51 Embedded tutorial: Code generation for embedded processors

Rainer Leupers

September 2000 **Proceedings of the 13th international symposium on System synthesis**

Full text available: pdf(62.34 KB) Additional Information: full citation, abstract, references

The increasing use of programmable processors as IP blocks in embedded system design creates a need for C/C++ compilers capable of generating efficient machine code. Many of today's compilers for embedded processors suffer from insufficient code quality in terms of

code size and performance. This violates the tight chip area and real-time constraints often imposed on embedded systems. The reason is that embedded processors typically show architectural features which are not well handled by class ...

52 System level modeling and verification: Embedded systems verification with FGPA-enhanced in-circuit emulator

M. Meerwein, C. Baumgartner, T. Wieja, W. Glauert

September 2000 **Proceedings of the 13th international symposium on System synthesis**

Full text available: pdf(109.43 KB) Additional Information: full citation, abstract, references, citings

In this paper we present a novel coverification concept for embedded microcontrollers that satisfies industrial requirements. Based on a commercially available CPU in-circuit emulator coupled with FPGA boards, it verifies the correctness of an implementation in terms of function and timing within a real-world environment.Using our system, the software engineer can write, test and optimize programs for a chip that is not yet physically existent. In addition the system is used to obtain software m ...

53 System level modeling and verification: Instruction-based system-level power evaluation of system-on-a-chip peripheral cores

Tony D. Givargis, Frank Vahid, Jörg Henkel

September 2000 **Proceedings of the 13th international symposium on System synthesis**

Full text available: pdf(109.80 KB) Additional Information: full citation, abstract, references, citings

Various system-level core-based power evaluation approaches for core types like microprocessors, caches, main memories, and buses, have been proposed in the past. Approaches for other types of components have been based either on the gate-level, register-transfer level, or behavioral-level. We propose a new technique, suitable for a variety of cores like peripheral cores, that is the first to combine gate-level power data with a system-level simulation model written in C++ or Java. For that purp ...

54 High-level library mapping for memories

Pradip K. Jha, Nikil D. Dutt

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(209.38 KB) Additional Information: full citation, abstract, references, citings, index terms

We present high-level library mapping, a technique that synthesizes a source memory module from a library of target memory modules. In this paper, we define the problem of high-level library mapping for memories, identify and solve the three subproblems associated with this task, and finally combine these solutions into a suite of two memory mapping algorithms. Experimental results on a number of memory-intensive designs demonstrate that our memory mapping approach generates a wide variety ...

Keywords: high-level synthesis, memory libraries, technology-mapping

55 Regression-based RTL power modeling

Alessandro Bogliolo, Luca Benini, Giovanni De Micheli

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(391.65 KB) Additional Information: full citation, abstract, references, citings, index terms

Register-transfer level (RTL) power estimation is a key feature for synthesis-based design flows. The main challenge in establishing a sound RTL power estimation methodology is the construction of accurate, yet efficient, models of the power dissipation of functional macros.

Such models should be automatically built, and should produce reliable average power estimates. In this paper we propose a general methodology for building and tuning RTL power models. We address both hard macros (presy ...

Keywords: RTL design, RTL power modeling, adaptive characterization, functional macros, regression models

56 Modeling and simulation of real defects using fuzzy logic
Amir Attarha, Mehradad Nourani, Carco Lucas
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(122.62 KB) Additional Information: full citation, abstract, references, index terms

Real defects (e.g. stuck-at or bridging faults) in the VLSI circuits cause intermediate voltages and can not be modeled as ideal shorts. In this paper we first show that the traditional zero-resistance model is not sufficient. Then, we present a resistive fault model for real defects and use fuzzy logic techniques for fault simulation and test pattern generation at the gate-level. Our method produces more realistic fault coverage compared to the conventional methods. The experimenta ...

57 A case study of synthesis for industrial-scale analog IP: redesign of the equalizer/filter frontend for an ADSL CODEC
Rodney Phelps, Michael J. Krasnicki, Rob A. Rutenbar, L. Richard Carley, James R. Hellums
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(211.88 KB) Additional Information: full citation, abstract, references, citings, index terms

A persistent criticism of analog synthesis techniques is that they cannot cope with the complexity of realistic industrial designs, especially system-level designs. We show how recent advances in simulation-based synthesis can be augmented, via appropriate macromodeling, to attack complex analog blocks. To support this claim, we resynthesize from scratch, in several different styles, a complex equalizer/filter block from the frontend of a commercial ADSL CODEC, and verify by full si ...

58 Self-test methodology for at-speed test of crosstalk in chip interconnects
Xiaoliang Bai, Sujit Dey, Janusz Rajski
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(113.37 KB) Additional Information: full citation, abstract, references, citings, index terms

The effect of crosstalk errors is most significant in high-performance circuits, mandating at-speed testing for crosstalk defects. This paper describes a self-test methodology that we have developed to enable on-chip at-speed testing of crosstalk defects in System-on-Chip interconnects. The self-test methodology is based on the Maximal Aggressor Fault Model [13], that enables testing of the interconnect with a linear number of test patterns. To enable self-testing of the interconnects, we h ...

59 Automatic test pattern generation for functional RTL circuits using assignment decision diagrams
Indradeep Ghosh, Masahiro Fujita
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(94.24 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present an algorithm for generating test patterns automatically from functional register transfer level (RTL) circuits that target detection of stuck-at faults in the circuit at the logic level. To do this we utilize a data structure named assignment decision

diagram which has been proposed previously in the field of high level synthesis. The advent of RTL synthesis tools have made functional RTL designs widely popular. This paper addresses the problem of test patt ...

60 Using general-purpose programming languages for FPGA design

Brad L. Hutchings, Brent E. Nelson

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(287.38 KB) Additional Information: full citation, abstract, references, citings, index terms

General-purpose programming languages (GPL) are effective vehicles for FPGA design because they are easy to use, extensible, widely available, and can be used to describe both the hardware and software aspects of a design. The strengths of the GPL approach to circuit design have been demonstrated by JHDL, a Java-based circuit design environment used to develop several large FPGA-based applications at several institutions. Major strengths of the JHDL environment include a common run-time for ...

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61 Efficient performance prediction for modern microprocessors
David Ofelt, John L. Hennessy
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Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, citings, index terms

62 Substrate crosstalk analysis in mixed signal CMOS integrated circuits: embedded tutorial
Makoto Nagata, Atsushi Iwata
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
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63 Optimal hardware pattern generation for functional BIST
Silvia Cataldo, Silvia Chiusano, Paolo Prinetto
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
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64 Automatic test bench generation for validation of RT-level descriptions: an industrial experience
F. Corno, M. Sonza Reorda, G. Squillero, A. Manzone, A. Pincetti
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65 Cycle-based simulation algorithms for digital systems using high-level decision diagrams (poster paper)
Adam Morawiec, Raimund Ubar, Jaan Raik
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R. Rosing, A. M. Richardson, A. P. Dorey
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67 Noise analysis of non-autonomous radio frequency circuits
Amit Mehrotra, Alberto L. Sangiovanni-Vincentelli
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68 Distributed simulation of VLSI systems via lookahead-free self-adaptive optimistic and conservative synchronization
Dragos Lungeanu, C.-J. Richard Shi
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Alfred V. Gomes, Abhijit Chatterjee
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70 Highlights of CMU research on CAD, CAM and CAT of VLSI circuits
John Paul Shen
November 1999 **Proceedings of 1986 fall joint computer conference on Fall joint computer conference**
Full text available: pdf(1.35 MB) Additional Information: full citation, references, index terms

71 Substrate modeling and lumped substrate resistance extraction for CMOS ESD/latchup circuit simulation
Tong Li, Ching-Han Tsai, Elyse Rosenbaum, Sung-Mo Kang
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72 MAELSTROM: efficient simulation-based synthesis for custom analog cells
Michael Krasnicki, Rodney Phelps, Rob A. Rutenbar, L. Richard Carley
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation conference**
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73 Enhancing simulation with BDDs and ATPG
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You-Sung Chang, Seungjong Lee, In-Cheol Park, Chong-Min Kyung
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76 Formal verification in hardware design: a survey
Christoph Kern, Mark R. Greenstreet
April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2
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77 SIGda '96, workshop: how do we expedite the commercial use of Ada?
Robert C. Leif
March 1999 **ACM SIGAda Ada Letters**, Volume XIX Issue 1
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78 HDL-based modeling of embedded processor behavior for retargetable compilation
Rainer Laupers
December 1998 **Proceedings of the 11th international symposium on System synthesis**
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79 Kernel Ada to unify hardware and software design
Sy Wong, Gertrude Levine
November 1998 **ACM SIGAda Ada Letters , Proceedings of the 1998 annual ACM SIGAda international conference on Ada**, Volume XVIII Issue 6
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80 A general approach for regularity extraction in datapath circuits
Amit Chowdhary, Sudhakar Kale, Phani Saripella, Naresh Sehgal, Rajesh Gupta
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